IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Xiaoju Wu, et al.	Docket No:	TI-31214
Serial No:	10/017,990	Conf. No:	8404
Examiner:	Dana Farahani	Art Unit:	2814
Filed:	12/14/2001		
For:	BIPOLAR JUNCTION TRANSISTOR WITH ELECTRICAL HOLE ISOLATOR		

APPEAL BRIEF UNDER 37 C.F.R. 1.192

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 8-12-03.

Ann Trent
Ann Trent

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed February 12, 2003, and the Advisory Action mailed May 7, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

On June 12, 2003, appellant appealed from the final rejection of claims 1-30.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

The appellant filed an amendment on April 11, 2003 arguing the validity of the examiner's final rejection of claims 1-30. In an office action dated May 7, 2003 the examiner indicated that the appellants argument did not place the application in condition for allowance.

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

A p-type substrate 22 is provided on which a n-type buried layer 24 is formed as shown in Figure 2(b) (page 6, lines 5-12). A p-type buried layer 26 is formed within the n-type buried layer 24 as shown in Figure 2(b). An epitaxial layer 30 is formed over the p-type buried layer followed by the formation of n-wells 32a and 32b in the epitaxial layer 30 (page 7, lines 8-17). Also shown in Figure 2(b) is the formation of the p-well 34 that may be formed either before or after the formation of the n-wells 32a and 32b (page 8, lines 6-10). As shown in Figure 3, isolation structures 36 are formed in the epitaxial layer 30. P-type regions 38 are formed in the p-well 34 to provide contact to the p-well region (page 11, lines 18-22) for the hole guard terminals HG_1. Contact is provided for the isolation terminals IS_2 to the n-well 32b through the n-type regions 42. A hole injector 52 is formed in the n-well 32a and can comprise any number of devices such as: (1) an output power device which gets forward biased when switching inductive loads; (2) a p-channel MOS transistor which can have forward biased its drain or source during the operation; (3) a power device operating at high current level, which tends to generate more holes; (4) any nodes connected to an input/output pin; (5) a power devices driving an inductive load in that during the switching of the states, the node will inject holes; and (6) any nodes connected to noisy digital power supply (page 11, lines 18-29, and page 12, lines 1-4). Various embodiments describing the biasing of the structure can be found on page 12, lines 18-29, and page 13, lines 1-19. In a specific example a transistor emitter region 40 and a transistor base region 44 can be formed in the n-well 32a (page 8, lines 11-23).

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

1. Are claims 1, 2, 4-6, 8, 13, 15, 17, 21-24, 27, 29, and 30 properly rejected under 35 U.S.C. 102(b) as being anticipated by Husher?

2. Are claims 3, 7, 10, 14, 25, 26, and 28 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 1, and further in view of Taniguch?

3. Are claims 9, 11, 12, 16, 18, 19, and 20 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 8, and further in view of S.M. Sze, Semiconductor Devices, Physics and Technology.

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 1-30 stand or fall together.

Arguments

Are claims 1, 2, 4-6, 8, 13, 15, 17, 21-24, 27, 29, and 30 properly rejected under 35 U.S.C. 102(b) as being anticipated by Husher?

Appellants maintain that claims 1, 2, 4-6, 8, 13, 15, 17, 21-24, 27, 29, and 30 are not properly rejected under 35 U.S.C. 102(b) as being anticipated by Husher.

Independent claim 1 of the instant invention is a claim to an electronic circuit. The electronic circuit comprises: a well formed in the first layer, wherein the well comprises a first conductivity type and has a side dimension and a bottom dimension; a first enclosure surrounding the side dimension and the bottom dimension of the well, wherein the first enclosure comprises a second conductivity type complementary of the first conductivity type and has a side dimension and a bottom dimension; and a second enclosure

surrounding the side dimension and the bottom dimension of the first enclosure, wherein the second enclosure comprises the first conductivity type.

In an office action dated 8/16/2002 the examiner described the Husher patent as containing a well 160 formed in the first layer. The examiner repeated this interpretation of the Husher patent in an office action dated 2/04/03. Furthermore in both office actions the examiner describes layer 150 in the Husher patent as a buried layer and directs the applicant to column 4, lines 53-56 to support this description. The examiner is correct in describing region 150 as a buried layer and this interpretation is supported by the relevant sections of the Husher patent described by the examiner. The examiner however is incorrect in describing the region labeled 160 in the Husher patent as a well. The proper description of the region labeled 160 is found in column 3, lines 67-68, and column 4, lines 1-2 of the Husher patent where is states, "P catch diffusion region 150 may be electrically connected, via annular P+ sinker region (or return region) 160, to the collector terminal of the transistor." Region 160 is therefore not a well region as incorrectly described by the examiner but is instead a sinker region as described in the Husher patent itself.

It is important to distinguish the established meaning of the words diffusion and well in the semiconductor arts. The word diffusion describes a physical phenomena used to form impurity regions in a semiconductor. The word well refers to a region that has a specific function and can be formed by a number of different methods including ion implantation, thermal diffusion etc. The word well in the semiconductor arts refers to a region formed in a semiconductor in which an electronic device is formed. A common example is a PMOS transistor formed in a n-well as part of a twin well CMOS process. As described on page 11, lines 24-29 and page 12, lines 1-7, the n-well region 32a can contain any number of electronic structures including: (1) an output power device which gets forward biased when switching inductive loads; (2) a p-channel MOS transistor which can have forward biased its drain or source during the operation; (3) a power device operating at high current level, which tends to generate more holes; (4) any nodes connected to an input/output pin; (5) a power devices driving an inductive load in that during the switching of the states, the node will inject holes; and (6) any nodes connected

to noisy digital power supply. It is therefore quite clear that in describing an electronic device the word well as used in claim 1 and buried layer and sinker as used in the Husher patent have specific and well established meanings in the semiconductor arts and are not equivalent.

Furthermore in an advisory action dated 5/7/2003 the examiner states, "although the Husher reference call region 160 a sinker region, it might as well be called a well region. A well region is nothing more than a diffusion region in a substrate." As described above many different regions can be formed using diffusion processes including well regions, source regions, drain regions, emitter regions, etc. Clearly there is no equivalence between a source region and an emitter region even though both regions may have been formed using diffusion processes. There is therefore no equivalency between the described sinker region in the Husher patent and the well region of claim 1 even though both regions may have been formed using diffusion processes.

The Husher patent therefore does not contain all the required elements of claim 1 of the instant invention and claim 1 is allowable over the cited art. Independent claim 22 contains the limitation of forming a well in the first layer. As described above the Husher patent does not describe a well region and therefore does not describing forming a well region. Independent claim 22 is therefore allowable over the cited art. Furthermore dependent claims 2, 4-6, 8, 13, 15, 17, and 21 depend from claim 1 and therefore contain the limitation of a well. Dependent claims 2, 4-6, 8, 13, 15, 17, and 21 are therefore allowable over the cited art. Dependent claims 23-24, 27, 29, and 30 depend from claim 22 and therefore contain the limitation of forming a well. Dependent claims 23-24, 27, 29, and 30 are therefore allowable over the cited art.

<u>Are claims 3, 7, 10, 14, 25, 26, and 28 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 1, and further in view of Taniguch</u>?

Appellant maintains that claims 3, 7, 10, 14, 25, 26, and 28 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher as applied to claim 1 in further view of Taniguchi.

As described above claim 1 is allowable over the Husher patent. The Taniguchi patent does not describe a well as required by the claims and therefore claims 3, 7, 10, 14, 25, 26, and 28 are allowable over the Husher patent in further view of Taniguchi.

Are claims 9, 11, 12, 16, 18, 19, and 20 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 8, and further in view of S.M. Sze, Semiconductor Devices, Physics and Technology?

Appellant maintains that claims 9, 11, 12, 16, 18, 19, and 20 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 8, and further in view of S.M. Sze, Semiconductor Devices, Physics and Technology?

As described above claim 1 is allowable over the cited art. Claim 8 depends on claim 1 and is also allowable over the prior art. Claims 9, 11, 12, 16, 18, 19, and 20 depend on claim 8 and are allowable over the cited art.

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1, 2, 4-6, 8, 13, 15, 17, 21-24, 27, 29 and 30 under 35 U.S.C. 102 and Claims 3, 7, 9, 10-12, 14, 16, 18-20, 25, 26 and 28 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper,

including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

Peter McLarty
Reg. No. 44,923
Attorney for Appellants

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-4258

APPENDIX

Claims on Appeal

1. An electronic circuit, comprising:

a semiconductor substrate;

a first layer in a fixed physical relation to the semiconductor substrate;

a well formed in the first layer, wherein the well comprises a first conductivity type and has a side dimension and a bottom dimension;

a first enclosure surrounding the side dimension and the bottom dimension of the well, wherein the first enclosure comprises a second conductivity type complementary of the first conductivity type and has a side dimension and a bottom dimension; and

a second enclosure surrounding the side dimension and the bottom dimension of the first enclosure, wherein the second enclosure comprises the first conductivity type.

2. The electronic circuit of claim 1:

wherein the well comprises a first well; and

wherein the first enclosure comprises:

a second well surrounding the side dimension of the first well; and

a buried layer adjacent the bottom dimension of the first well.

3. The electronic circuit of claim 2 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

4. The electronic circuit of claim 2:

wherein the buried layer comprises a first buried layer; and

wherein the second enclosure comprises:

a third well surrounding a side dimension of the second well; and

a second buried layer adjacent a bottom dimension of the first buried layer.

5. The electronic circuit of claim 4:

wherein the first layer comprises an epitaxial layer; and

wherein the first and second buried layers are formed in the substrate.

6. The electronic circuit of claim 5:

wherein the second and third wells are formed in the epitaxial layer.

7. The electronic circuit of claim 6 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

8. The electronic circuit of claim 6:

wherein the first well comprises circuitry operable to emit electrical holes in response to an operating voltage that may swing between a predetermined low voltage and a predetermined high voltage;

and further comprising:

a first terminal for applying a voltage potential to the first enclosure; and

a second terminal for applying a voltage potential to the second enclosure.

9. The electronic circuit of claim 8 and further comprising circuitry for connecting the first terminal to the second terminal.

10. The electronic circuit of claim 9 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

11. The electronic circuit of claim 10 and further comprising circuitry for connecting the first terminal and the second terminal to the predetermined low voltage.

12. The electronic circuit of claim 10 and further comprising:

circuitry for connecting the first terminal to the predetermined low voltage; and

circuitry for connecting the second terminal to the predetermined high voltage.

13. The electronic circuit of claim 6:

wherein the first enclosure comprises a transistor collector;

wherein the first well comprises a transistor base;

and further comprising a transistor emitter formed as a region within the first well.

14. The electronic circuit of claim 13 wherein the transistor comprises a vertical PNP transistor.

15. The electronic circuit of claim 14:

wherein the transistor collector is operable in response to an operating voltage that may swing between a predetermined low voltage and a predetermined high voltage;

and further comprising a terminal for applying a voltage potential to the second enclosure.

16. The electronic circuit of claim 15 and further comprising circuitry for connecting the terminal to the predetermined high voltage.

17. The electronic circuit of claim 4:

wherein the first well comprises circuitry operable to emit electrical holes in response to an operating voltage that may swing between a predetermined low voltage and a predetermined high voltage;

and further comprising:

a first terminal for applying a voltage potential to the first enclosure; and

a second terminal for applying a voltage potential to the second enclosure.

18. The electronic circuit of claim 17 and further comprising circuitry for connecting the first terminal to the second terminal.

19. The electronic circuit of claim 18:

wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type;

and further comprising circuitry for connecting the first terminal and the second terminal to the predetermined low voltage.

20. The electronic circuit of claim 18:

wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type;

and further comprising:

circuitry for connecting the first terminal to the predetermined low voltage; and

circuitry for connecting the second terminal to the predetermined high voltage.

21. The electronic circuit of claim 4:

wherein the first enclosure comprises a transistor collector;

wherein the first well comprises a transistor base;

and further comprising a transistor emitter formed as a region within the first well.

22. A method of forming an electronic circuit, comprising the steps of :

forming a first layer in a fixed physical relation to a semiconductor substrate;

forming a well formed in the first layer, wherein the well comprises a first conductivity type and has a side dimension and a bottom dimension;

forming a first enclosure surrounding the side dimension and the bottom dimension of the well, wherein the first enclosure comprises a second conductivity type complementary of the first conductivity type and has a side dimension and a bottom dimension; and

forming a second enclosure surrounding the side dimension and the bottom dimension of the first enclosure, wherein the second enclosure comprises the first conductivity type.

23. The method of claim 22:

wherein the well comprises a first well; and

wherein the step of forming first enclosure comprises the steps of:

forming a second well surrounding the side dimension of the first well; and

forming a buried layer adjacent the bottom dimension of the first well.

24. The method of claim 23 wherein the step of forming a buried layer occurs prior to the step of forming the well.

25. The method of claim 23 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

26. The method of claim 25 wherein the step of forming a buried layer comprises implanted at a dosage on the order of $5e^{15}/cm^2$ and at an energy on the order of 60 keV.

27. The method of claim 25:

wherein the buried layer comprises a first buried layer; and

wherein the step of forming a second enclosure comprises the steps of:

forming a third well surrounding a side dimension of the second well; and

forming a second buried layer adjacent a bottom dimension of the first buried layer.

28. The method of claim 27 wherein the step of forming a second buried layer comprises implanted at a dosage on the order of $8e^{13}/cm^2$ and at an energy on the order of 60 keV.

29. The method of claim 27 wherein the step of forming a second buried layer occurs prior to the step of forming the third well and prior to the step of forming the second well.

30. The method of claim 22:

wherein the first enclosure comprises a transistor collector;

wherein the first well comprises a transistor base;

and further comprising the step of forming a transistor emitter as a region within the well.